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NOTICE OF ALLOWANCE AND FEE(S) DUE

24737 7590 03/10/2010

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> 2183 DATE MAILED: 03/10/2010

EXAMINIER
PETRANEK, JACOB ANDREW
ART UNIT PAPER NUMBER

APPLICATION NO. FILING DATE FIRST NAMIGD INVENTOR ATTORNEY DOCKET NO. CONFIRMATION NO.

10561,454 122020005 Carlos Antonio Alba Pinto NL 030726 6437

TITLE GO FINENTION: DATA PROCESSING DEVICE WITH INSTRUCTION CONTROLLED CLOCK SPEED

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	06/10/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

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If the SMALL ENTITY is shown as NO:

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II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450

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							(Date)
APPLICATION NO.	FILING DATE		FIRST NAMED INVENTOR		ATTC	RNEY DOCKET NO.	CONFIRMATION NO.
10/561,454	12/20/2005		Carlos Antonio Alba Pinto			NL 030726	6437
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APPLN, TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE	3 FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0		\$1810	06/10/2010
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PETRANEK, JA		2183	712-214000 2. For printing on the p				
1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.563). Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. The Address from PTO/SB/122 attached. The Address' indication (or "Fee Address" indication form PTO/SB/147; Rev 0.30 c or more recent) attached. Use of a Customer PTO/SB/147; Rev 0.30 c or more recent) attached. Use of a Customer Number is required. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON			or agents OR, alternative (2) the name of a single registered attorney or a 2 registered patent attorney issued, no name will be	name of a single firm (having as a member a ed attorney or agent) and the names of up to errord patent attorneys or agents. If no name is no name will be printed.			
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- 11	s SMALL ENTITY state	is. See 37 CFR 1.27.	b. Applicant is no long				
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PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.



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PHILIPS INTELLECTUAL PROPERTY & STANDARDS			PETRANEK, JACOB ANDREW		
P.O. BOX 3001			ART UNIT	PAPER NUMBER	
BRIARCLIFF MANOR, NY 10510		2183			

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 603 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 603 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Application No. Applicant(s) 10/561,454 ALBA PINTO ET AL. Notice of Allowability Examiner Art Unit 2183 Jacob Petranek -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308. This communication is responsive to appeal brief filed on 12/16/2009. The allowed claim(s) is/are 1-2,4-8,10-12. 3. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). b) ☐ Some* c) ☐ None of the: a) \square All 1. T Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)). * Certified copies not received: _____. Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient. CORRECTED DRAWINGS (as "replacement sheets") must be submitted. (a) Including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached 1) Inhereto or 2) In to Paper No./Mail Date (b) including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d). 6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

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- Notice of References Cited (PTO-892)
- Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3. Information Disclosure Statements (PTO/SB/08),
- Paper No./Mail Date _____
- Examiner's Comment Regarding Requirement for Deposit of Biological Material
- 5. ☐ Notice of Informal Patent Application
- Interview Summary (PTO-413), Paper No./Mail Date .
- 7. Examiner's Amendment/Comment
- 8. X Examiner's Statement of Reasons for Allowance
- 9. Other ____.
 /Jacob Petranek/

/Jacob Petranek/ Examiner, AU 2183 Application/Control Number: 10/561,454 Page 2

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EXAMINER'S AMENDMENT

 An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Robert M. McDermott on 3/5/2010.

The application has been amended as follows:

Change claim 1 line 3 to:

an instruction issue unit_that is [[configure(Previously presented) d]] configured to issue

Change claim 4 line 4 to:

involved in producing a result from the second functional unit_during execution of the

REASONS FOR ALLOWANCE

- 1. The following is an examiner's statement of reasons for allowance:
- 2. Applicant argues "The Office action asserts that one of skill in the art would apply Sager's teachings to Sih's architecture "for the advantage of decreased chip space usage and power savings". This assertion is incorrect. Sager achieves this decreased chip space usage and power savings by reducing the design constraints on the elements in the outer clock domains, off the critical path. Using smaller transistors will reduce chip space, but also increase transition time for driving a given load; a reduced clock rate will accommodate this increased transition time and consume less power. That is, the savings achieved by Sager are achieved at the cost of increased delay time,

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and this increased delay time is permitted because it is applied to the latency-tolerant elements that are off the critical path in the outer clock domains.

Given that the purpose of Sih's design is to provide high-speed MAC operations, one of skill in the art would optimize all of the elements along the critical path subject to a given set of design constraints. One of skill in the art would not be motivated to apply techniques that only provide an advantage for latency-tolerant elements to Sih's latency-intolerant multiply, shift, and add elements, as asserted by the Examiner. If a slower instruction cycle rate were acceptable, one of skill in the art would design all of Sih's multiply, shift, and add elements to operate at this slower instruction cycle rate, because it would then be the most efficient in area and power consumption for the given instruction cycle rate. Sager's degradation of speed for selective elements would be a sub-optimal design compared to a consistent degradation of speed for all elements in series along the critical path.

Because there is no apparent reason to apply Sager's teachings to the multiply, shift, add elements of Sin, as asserted by the Examiner, and because the application of Sager's teachings to these elements would be unsatisfactory for Sin's intended purpose, the applicants respectfully maintain that the rejection of claims 1-2, 4-8, and 10-11 under 35 U.S.C. 103(a) over Sin, Hennessey, and Sager is unfounded, and should be withdrawn."

The Examiner agrees for the following reasons. The rejection used the combination of Sih and Sager to teach the claimed limitation of varying the rate of clocking when the instruction sequence includes instructions of the second type. The rejection used the MAC instructions that would execute only on a single MAC operating path as instructions of the first type and the dual-MAC instructions that would execute on two MAC operating paths as instructions of the second type. Thus, the dual-MAC instructions would have a clock rate that varied from the normal processor clock rate when executed. The rejection placed the circuitry for executing the dual-MAC operations of Sih on the latency tolerant sub-core and the circuitry of the MAC operations of Sih on the latency intolerant sub-core. However, the Examiner agrees with the applicant that there isn't sufficient motivation as to why one would add the dual-MAC and MAC functionality to each of the respective sub-cores. Adding the dual-MAC to the slower subcore somewhat defeats the purpose of having the dual-MAC

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functionality because Sih uses this extra dedicated hardware to speed up frequently used functions (column 1 lines 49-55). Additionally, splitting the operations into separate sub-cores would require duplication of hardware logic, which would lead to increased chip space and power consumption.

Additionally, if the combination hypothetically placed the dual-MAC functionality into the latency intolerant sub-core, then there would be no need to place the slower MAC functionality into the latency tolerant sub-core. This is because the intolerant sub-core's clock rate would be more than sufficient to execute MAC operations if the clock rate can also execute dual-MAC operations. Thus, it would make no sense to one of ordinary skill in the art to place the MAC functionality on the tolerant core if the dual-MAC functionality is placed on the intolerant core.

As there is not proper motivation to combine the Sager reference with the Sih reference, the combination has been withdrawn and the independent claims are now in condition for allowance. An after-final amendment was entered that corrected the claim objection for claim 12 that resulted in the withdrawal of the claim objection. Additionally, the drawing objection has also been withdrawn. Thus, the case is now in condition for allowance as all claims are allowable and there are no outstanding objections.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jacob Petranek/ Examiner, AU 2183